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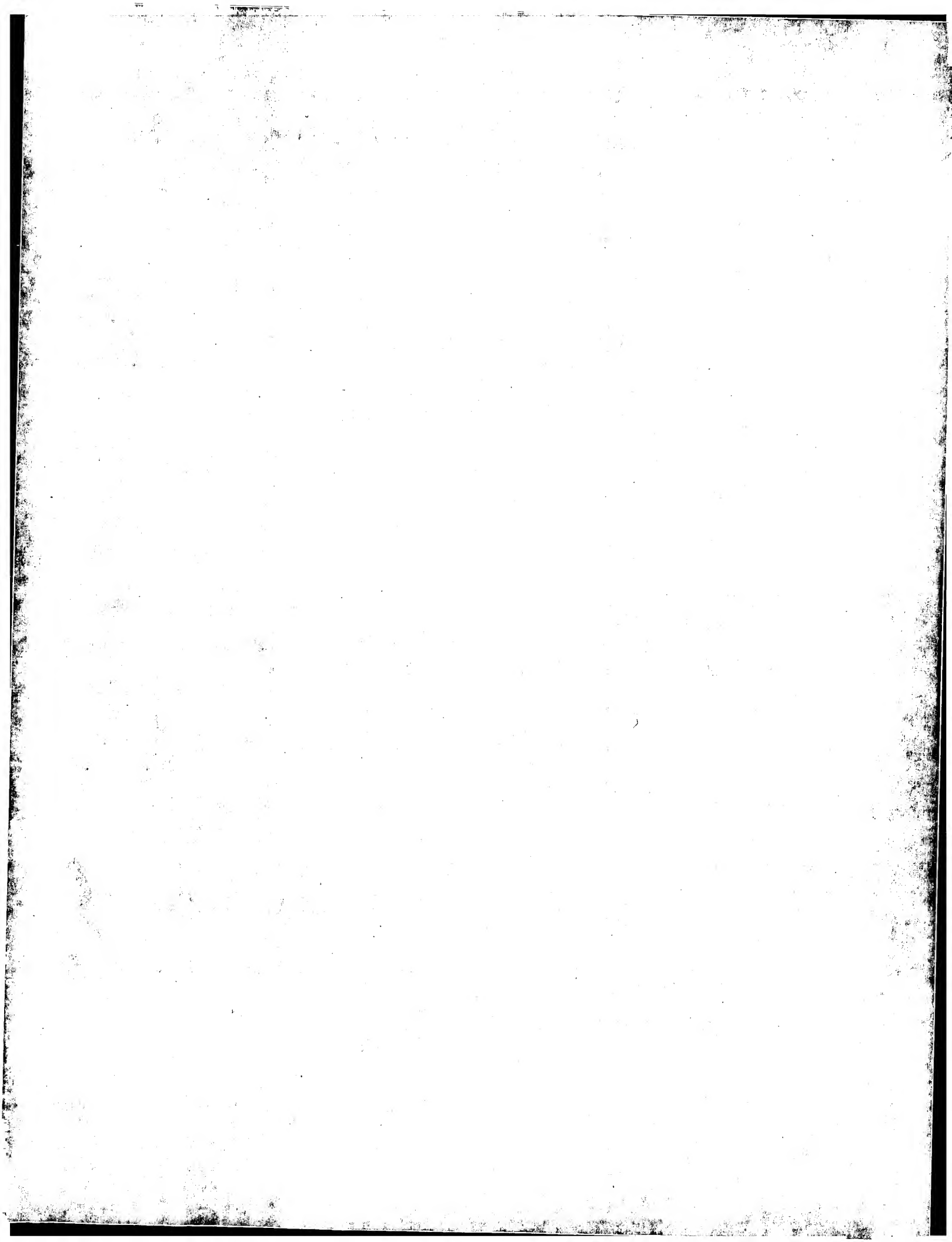
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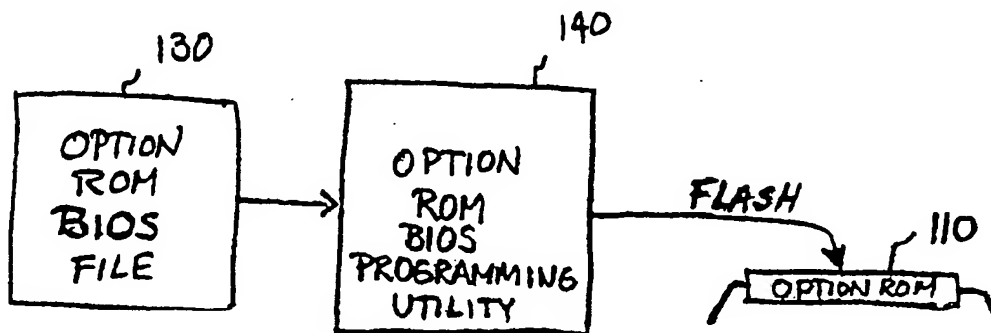
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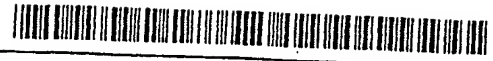
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(54) Title: **METHOD FOR FLASHING A READ ONLY MEMORY (ROM) CHIP OF A HOST ADAPTER WITH UPDATED BIOS CODE**



(57) Abstract: A programming method (140) for flashing a read only memory (ROM) chip (110) of a host adapter (106) with an updated BIOS code (130) is provided. The method includes building a table having start address information and memory size information of memory space occupied in the system random access memory (RAM) (120) by one or more PCI host adapters connected thereto. The method further includes identifying a selected PCI host adapter (106) having a ROM chip (110). A desired amount of memory space for an updated option ROM code (130) is mapped between the system RAM (120) and the ROM chip (110). A start address in RAM (120) of an additional PCI host adapter that is determined to lie within the desired amount of memory space is redirected. The method further includes loading the updated option ROM code (130) into the desired amount of memory space in RAM (120) and in the ROM chip (110) of the selected host adapter (106).

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## METHOD FOR FLASHING A READ ONLY MEMORY (ROM) CHIP OF A HOST ADAPTER WITH UPDATED BIOS CODE

5

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

This invention relates generally to computers systems, and more particularly to the updating of computer code implemented to boot up a computer system.

#### 10 2. Description of the Related Art

Today's personal computer systems provide users with a high degree of flexibility in terms of the number of peripheral devices that may be connected to a given system. For instance, users are able to connect additional internal and external peripheral devices to meet the storage or data access demands required to complete the user's job. Such peripheral  
15 devices can include internal or external hard drives, compact disc (CD) players, digital video disc (DVD) players, compact disc recordables (CD-Rs), etc.

To meet the connection needs for these peripheral devices, most computers have IDE connectors and PCI connectors built into the computer's motherboard. Typically, the IDE connectors are used to connect internal devices, such as, hard drives and CD-ROM drives.  
20 The PCI connectors are generally configured to receive host adapter cards, which allow the connection of both internal and external devices. As is well known, there are numerous types of host adapters, some of the most commonly used are SCSI host adapters, redundant array of inexpensive disk (RAID) host adapters, and the like. SCSI host adapters are one of the most popular adapters due to peripheral device arrangement flexibility and performance. For  
25 instance, one SCSI host adapter can serve as the communication link for up to 15 internal and external peripheral devices.

Most host adapters have option ROM chips integrated onto the printed circuit board of the host adapter card. The option ROM chip is typically an electrically erasable programmable read only memory (EEPROM), which stores program instructions that are used during the boot process of the computer system that has the host adapter card connected thereto. Without these program instructions, the host adapter card and any of the peripheral devices connected to the host adapter card will not be able to communicate with the host computer system, and thus, will be rendered useless. From time to time, the manufacturers of these host adapters find it useful to update the program instructions that are resident in the option ROM chips. Unfortunately, because more than one host adapter card may be connected to a particular computer system, this updating can become problematic in view of the limited space available in the system RAM for this function.

To further elaborate on this problem, it is useful to generally understand the booting process of a computer system having PCI host adapters connected thereto. During bootup, the system BIOS will assign each PCI host adapter to certain memory space in the system RAM. This memory space is used to enable the computer's operating system to communicate with particular registers that are resident on the PCI host adapter card. In general, the system RAM will ask each host adapter to identify how much RAM memory space it needs, and then, that space is allocated. It should be noted that there is only a fixed range of memory space that can be used for PCI devices. A further complication is that different computer manufacturers utilize different system BIOS, which allocate the available RAM memory space in different ways. Accordingly, the memory address location allocated for a given PCI device by one system BIOS may well be different if it is allocated by a system BIOS of another manufacturer.

In order to effectuate an update of the program instructions of a given option ROM chip, the host adapter containing the desired option ROM chip is identified. To update these

program instructions, the entire contents of the program instructions also have to be written to the system RAM. in the same location that was previously allocated for the host adapter. Because program instruction updates continue to provide added functionality or operate to fix errors in existing code, the size of the update can be quite large. The problem here is, that the  
5 new code may be of a size that it may require memory space that is already occupied by other PCI devices. When this occurs, the update will not be made because there will be no space available in the system RAM. As can be appreciated, there are many reasons why there is a need to update the code in option ROMs, and if this updating is not possible, the computer user can lose some or fail to utilize all of the functionality provided by the peripheral devices  
10 that are connected to the host adapter.

In view of the foregoing, there is a need for a method and computer code utility for programming code updates into option ROM chips of host adapters.

### SUMMARY OF THE INVENTION

15 Broadly speaking, the present invention fills these needs by providing a computer implemented method for programming option ROM chips with updated code utilizing a free space memory allocation utility. The free space memory allocation utility is configured to intelligently redirect start address of memory space previously allocated by other host adapters which lie in memory space needed by the updated code. Once the updated code is  
20 flashed to the desired option ROM chip, the redirected start address are restored. It should be appreciated that the present invention can be implemented in numerous ways, including as a process, an apparatus, a system, computer readable media, or a device. Several inventive embodiments of the present invention are described below.

In one embodiment, a programming method for flashing a read only memory (ROM)  
25 chip of a host adapter with an updated BIOS code is disclosed. The host adapter is connected

to a host computer system. The method includes building a table having start address information and memory size information of memory space occupied in the random access memory (RAM) of the host computer system by one or more PCI host adapters which are connected to the computer system via a PCI bus. The method then moves to identifying a  
5 selected PCI host adapter having a ROM chip. A desired amount of memory space for an updated option ROM code is then mapped between the RAM of the host computer system and the ROM chip. Now, a start address in RAM of an additional PCI host adapter that is determined to lie within the desired amount of memory space is redirected. Preferably, the redirection is temporarily made to zero. The method now moves to loading the updated  
10 option ROM code into the desired amount of memory space in RAM and in the ROM chip of the selected host adapter. In this preferred embodiment, the method also includes restoring the start address in RAM of the additional PCI host adapter after the loading of the updated option ROM code is complete. If there is more than one host adapter occupying space in the desired amount of memory space, each of the start addresses of those host adapters is also  
15 temporarily redirected to zero while the loading is performed.

In another embodiment, a method for programming a read only memory (ROM) chip of a host adapter that is connected to a computer system is disclosed. The method includes:  
(a) scanning for PCI host adapters that are connected to the computer system; (b) building a table having start address information and memory size information of memory space  
20 occupied in random access memory (RAM) by the PCI host adapters; (c) identifying a selected PCI host adapter having a ROM chip that is configured to be programmed with an updated option ROM code, such that the selected PCI host adapter is associated with a selected start address and a selected memory size; (d) mapping a desired amount of memory space for the updated option ROM code from RAM to the ROM chip; (e) identifying ones of  
25 the PCI host adapters having memory space in RAM in the desired amount of space



beginning with the selected start address and extending for an update memory size; (f) redirecting start addresses of the ones of the PCI host adapters lying within the desired amount of space in RAM; and (g) loading the updated option ROM code into the desired amount of space in RAM and into the ROM chip.

5           In still a further embodiment, programming utility having program instructions for flashing a read only memory (ROM) chip of a host adapter with an updated BIOS code is disclosed. The host adapter is connected to a host computer system. The programming utility includes: (a) program instructions for building a table having start address information and memory size information of memory space occupied in the random access memory  
10 (RAM) of the host computer system by one or more PCI host adapters which are connected to the computer system via a PCI bus; (b) program instructions for identifying a selected PCI host adapter having a ROM chip; (c) program instructions for mapping a desired amount of memory space for an updated option ROM code between the RAM of the host computer system and the ROM chip; (d) program instructions for redirecting a start address in RAM of  
15 an additional PCI host adapter that is within the desired amount of memory space; and (e) program instructions for loading the updated option ROM code into the desired amount of memory space in RAM and in the ROM chip of the selected host adapter. Preferably, the utility also includes program instructions for restoring the start address in RAM of the additional PCI host adapter after the loading of the updated option ROM code is complete.

20           In yet another embodiment, a method for flashing a read only memory (ROM) chip with an updated BIOS code is disclosed. The method includes: (a) building a table having start address information and memory size information of memory space occupied in a random access memory (RAM) of a host computer system by one or more host adapters which are connected to the host computer system; (b) identifying a selected host adapter

having a ROM chip; (c) mapping a desired amount of memory space for an updated option ROM code between the RAM of the host computer system and the ROM chip; (d) redirecting a start address in RAM of an additional host adapter that is within the desired amount of memory space; and (e) loading the updated option ROM code into the desired amount of memory space in RAM and in the ROM chip of the selected host adapter.

Other aspects and advantages of the invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

The present invention will be readily understood by the following detailed description in conjunction with the accompanying drawings, and like reference numerals designate like structural elements.

Figure 1A shows a block diagram of a host computer system having a plurality of host adapters connected thereto.

Figure 1B illustrates a more detailed view of a host adapter card being connected to a PCI bus, and communicating with a system bus and RAM.

Figure 2 illustrates a more detailed diagram of a system RAM having allocated memory space, in accordance with one embodiment of the present invention.

Figure 3 illustrates a simplified block diagram of an updating operation of the option ROM BIOS code resident on one of the ROM chips of a host adapter, in accordance with one embodiment of the present invention.

Figure 4 illustrates another example of the system RAM having allocated memory space, in accordance with one embodiment of the present invention.

Figure 5 illustrates a flowchart that describes the method operations of updating the option ROM BIOS of a selected option ROM chip, in accordance with one embodiment of the present invention.

Figure 6 illustrates in more detail the intelligent free space allocation performed during an operation of Figure 5, in accordance with one embodiment of the present invention.

Figures 7A and 7B illustrate tables having allocated memory starting addresses and sizes for host adapters, in accordance with one embodiment of the present invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

An invention is described for a computer implemented method for programming option ROM chips with updated code utilizing a free space memory allocation utility. The free space memory allocation utility is configured to intelligently redirect start address of memory space previously allocated by other host adapters which lie in memory space needed by the updated code. Once the updated code is flashed to the desired option ROM chip, the redirected start address are restored. It will be obvious, however, to one skilled in the art, that the present invention may be practiced without some or all of these specific details. In other instances, well known process operations have not been described in detail in order not to unnecessarily obscure the present invention.

As an overview, the option ROM BIOS programming utility of the present invention is configured to scan all PCI devices in the system and obtain their allocated PCI memory ranges. From this information, it is possible to determine if there will be enough memory space available for the updated option ROM code without clashing with other PCI devices. If it is determined that a clash will occur, then memory access with the clashing PCI devices

will be temporarily disabled by re-mapping the base address registers. When the update has been flashed to the option ROM chip and the intelligently allocated memory space in RAM, the base address registers of the clashing PCI devices will be restored to the pre-re-mapping state, and the system will go back to normal operation. Figures 1A through 7B will now be  
5 described to more fully describe the details of the present invention.

Figure 1A shows a block diagram 100 of a host computer system 102 having a plurality of host adapters 106 connected thereto. In general, the host computer system 102 typically has a plurality of PCI connectors built into the motherboard to allow different types of host adapters to be connected to a PCI bus of the host computer system. In this example,  
10 a host adapter (HA<sub>1</sub>) 106a, a host adapter (HA<sub>2</sub>) 106b, a host adapter (HA<sub>3</sub>) 106c, and a host adapter (HA<sub>4</sub>) 106d are connected to the host computer system 102.

Each of the host adapters 106 typically has a controller chip 108, and a ROM chip 110 integrated to the printed circuit board of the host adapter. Of course, the host adapter card 106 will also include other supporting circuitry that will enable appropriate execution  
15 and communication with the host computer system 102. As shown in Figure 1B, the host adapter 106 can be a SCSI host adapter that can provide appropriate communication for one or more peripheral devices 107, which may be SCSI peripheral devices. The peripheral device 107 communicates via an appropriate link 109, which may be an internal ribbon connection or an external cable. The host adapter 106 is shown connected to a PCI bus 114  
20 via a PCI connector 112. The PCI bus 114 typically communicates through a bus bridge 116 to the system bus 118 of the host computer system 102. The system bus 118 also provides a communication path to the system RAM 120.

During the boot-up process of the host computer system 102, the system BIOS is configured to initialize each of the host adapters 106 to enable appropriate communication

between the host computer system 102 and associate peripheral devices 107. To effectuate the initialization, the system BIOS will allocate a certain amount of communication memory space in the system RAM 102 for each of the host adapter cards 106a.

Figure 2 illustrates a more detailed diagram of the system RAM 120, in accordance with one embodiment of the present invention. As shown, the system RAM 120 utilizes different address ranges for processing different tasks. For instance, memory space 120a is typically used for operating system (OS) programs and operating system files. An address range 120b is typically used for the various host adapters 106 that may be connected to the host computer system 102.

In general, during the initialization by the system BIOS, the system BIOS will allocate a certain amount of memory space in the system RAM 120 to establish communication with the register chip set on each of the host adapters. This memory space will therefore allow the operating system (OS) to communicate with the host adapters connected to the host computer system 102.

In more detail, the address range 120b shows four distinct address ranges 206a, 206b, 206c, and 206d for the host adapters HA<sub>1</sub>, HA<sub>2</sub>, HA<sub>3</sub>, and HA<sub>4</sub>, respectively. Each of the address ranges will have an associated start address, which are shown as SA<sub>1</sub>, SA<sub>2</sub>, SA<sub>3</sub>, and SA<sub>4</sub>. The address ranges 206 will also have an associated size parameter, which are shown as SIZE<sub>1</sub>, SIZE<sub>2</sub>, SIZE<sub>3</sub>, and SIZE<sub>4</sub>.

As mentioned above, the actual allocated location space within the address range 120b for each of the host adapters will vary depending upon the particular system BIOS that is initializing the host adapters 106. That is, different system BIOS manufacturers will have different ways of allocating this memory space. Accordingly, the actual address ranges 206 for each of the host adapters 106 will vary in different systems.

Figure 3 illustrates a simplified block diagram of an updating operating of the option ROM BIOS code resident on one of the ROM chips 110 of a host adapter 106. For instance, it may be necessary to update the BIOS program resident on in one of the ROM chips 110 of a host adapter 106. To accomplish this, the user will typically obtain an updated option ROM BIOS file 130 that needs to be programmed into an existing option ROM chip 110 of one of the host adapter 106. As such, the ROM chips 110 are programmable chips, such as electrically erasable programmable read only memories (EEPROMs) that can be flashed with a new updated program.

In this preferred embodiment, the option ROM BIOS file 130 is flashed into the option ROM chip 110 using an option ROM BIOS program utility 140. The option ROM BIOS programming utility 140 is configured to allow the flashing of the updated option ROM BIOS file 130 into the option ROM 110 even in situations where there is not enough space the system RAM 120. In general, the option ROM BIOS program utility 140 will be configured to dynamically and intelligently allocate enough memory space in the system RAM 120 regardless of the number of host adapters 106 that have previously been allocated memory space in the memory space 120b of the system RAM 120.

By way of example, if the updated option ROM BIOS file is about 64K in size, and the update is mapped to the option ROM chip 110 of the host adapter  $HA_j$ , the system BIOS will need to write the 64K of the update in a location that begins at the starting address  $SA_j$  (i.e.,  $SA_j$  is associated with the starting address of host adapter  $HA_j$ ). However, the size of the update is larger than the size of the current allocated memory space in address range 206c. In this example, the new address range will occupy an address range 206c'. When this occurs, the amount of memory space required for the update in the system RAM 120 will overlap the area which is occupied by the address range 206d and is associated with the

host adapter HA<sub>j</sub>. This will, of course cause a conflict that can have the potential of crashing or hanging-up the computer system.

In order to intelligently allocate memory space for the updated option ROM BIOS file 130, the option ROM BIOS program utility 140 is configured to redirect the starting address of the host adapter HA<sub>j</sub> for a period of time that allows writing of the entire update in the address range 206c'. At about the same time the update is written to the system RAM 120, the update will also be flashed to the option ROM 110, via a mapping operation. The option ROM BIOS programming utility 104, therefore assists in performing the redirection of the starting address of any address ranges 206 associated with host adapters that may be in the range of the update. Accordingly, although this example only illustrates a case where one address range is conflicting, in cases where the system RAM is more crowded, all starting addresses of conflicting address ranges will be temporarily redirected. Preferably, the starting addresses are temporarily redirected to zero.

Figure 5 illustrates a flowchart 400 that describes the method operations of updating the option ROM BIOS of a selected option ROM chip 110, in accordance with one embodiment of the present invention. The method begins at an operation 402 where a set of host adapters are provided. In general, a host computer system 102 can have a number of host adapters, each of which are connected to the motherboard of the host computer system 102, via a PCI bus, for example. Once a set of host adapters are provided in operation 402, the method advances to an operation 404 where the host computer system is booted up.

Now the method moves to operation 406 where the system BIOS will scan the PCI bus of the host computer system to identify each of the host adapters that are part of the provided set of host adapters. The method then advances to operation 408 where the system BIOS allocates communication memory space (*i.e.*, address ranges 206), in the system RAM

of the host computer system. As mentioned above, the actual location of the address ranges associated with the communication memory space will be different depending upon the manufacturer of the system BIOS. The standard boot procedure is then complete at operation 410 and the method proceeds to an operation 412 where the user may desire to  
5 update the option ROM code in one of the host adapters.

In the example of Figure 4, suppose that host adapter HA<sub>3</sub> is selected to have its option ROM code updated. Once the user selects the desired option ROM chip 110 of host adapter HA<sub>3</sub>, the method proceeds to operation 414 where an update option ROM code and a utility for flashing the updated option ROM code is obtained. By way of example, the  
10 updated option ROM code and the utility for flashing the updated option ROM code can be obtained by way of a floppy disk, a CD-ROM, over a computer network, or over the Internet. Once the desired updated option ROM code and the utility for flashing the updated option ROM code are obtained, the method will move to an operation 416 where the utility is run to dynamically identify an amount of free space in the system RAM.

15 In this embodiment, the amount of free space is configured to receive the update option ROM code. The method now advances to an operation 418 where the amount of free space in the system RAM is mapped to the option ROM chip (e.g., flash option ROM chip) on the selected host adapter that is configured to receive the updated option ROM code. Now, the method will move to an operation 420 where the updated option ROM code is  
20 loaded to the mapped amount of free space, so that the option ROM code is stored in both the system RAM and the option ROM chip of the desired host adapter. Once the update has been loaded, the method will advance to an operation 422 where the computer system is preferably rebooted so that the selected host adapter can operate implementing its updated option ROM code.



Figure 6 illustrates in more detail the intelligent free space allocation performed during operation 418 of Figure 5, in accordance with one embodiment of the present invention. As mentioned above, because updates of the option ROM code are many times going to be larger than the allocated communication memory space 206, there is a good chance that the address range necessary for the update in the system RAM 120 will already have been taken up by another host adapter. Accordingly, the intelligent free space allocation of the present invention begins at an operation 450, where all PCI devices (*i.e.*, host adapters) that are connected to the computer system are scanned.

After the scanning is complete, a table having start addresses and size requirements in the system RAM for each of the PCI devices is created in operation 452. For instance, Figure 7A illustrates an example where four host adapters HA<sub>1</sub> through HA<sub>4</sub> have been scanned and each will have an associated start address SA<sub>1</sub> through SA<sub>4</sub>, as well as size requirements SIZE<sub>1</sub> through SIZE<sub>4</sub>. After this table has been built in operation 452, the method will proceed to an operation 454 where a start address and size of the selected host adapter that is configured to be flashed with the updated option ROM code is located. In this example, host adapter HA<sub>3</sub> is the selected host adapter, and it will have an associated start address SA<sub>3</sub> and a SIZE<sub>3</sub> (*i.e.*, an address range). At this point, the method will proceed to a decision operation 456 where it is determined whether the update has available RAM space beginning with start address SA<sub>3</sub>.

In the example of Figure 4, it is evident that the address range 206c' does not have enough free space available for the updated option ROM code. As such, the method will proceed to an operation 458 where reference is made to the table built in operation 452 in order to identify the PCI devices that fall within the space required by the update option ROM code. Once again, in Figure 4, host adapter HA<sub>1</sub> is taking up communication memory

space starting at start address  $SA_i$ . Accordingly, the method will proceed to an operation 460 where the start addresses of any of the PCI devices that fall within the space required by the updated option ROM code are identified.

At this point, the start code address of the devices that were identified to fall within the space required by the updated option ROM code are redirected. By way of example, Figure 7B illustrates the table 302 in which the start address of host adapter  $HA_i$  is set to zero so that the updated option ROM code can be written beginning at start address  $SA_i$ . In one particular example, the updated option ROM code may be 64K, and all 64K will now be able to be written to the system RAM 120 as well as the option ROM chip 110 in accordance with the mapped amount of free space as described with reference to operation 420.

On the other hand, if it was determined in operation 456 that there is available space in the system RAM for the updated option ROM BIOS code, then the method would directly move to operation 420 from decision operation 456. In the same manner, when the updated option ROM code is loaded, that same option ROM code will be written (i.e., mapped) to both the system RAM 120 and the option ROM chip 110. After the updated option ROM code has been appropriately loaded to the mapped amount of free space to both the system RAM 120 and the option ROM chip 110, the option ROM BIOS program utility 140 will restore the start addresses of the host adapters that were conflicting with the updated option ROM code memory space range.

The invention may also employ various computer-implemented operations involving data stored in computer systems. These operations are those requiring physical manipulation of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and

otherwise manipulated. Further, the manipulations performed are often referred to in terms, such as producing, identifying, determining, or comparing.

Any of the operations described herein that form part of the invention are useful machine operations. The invention also relates to a device or an apparatus for performing these operations. The apparatus may be specially constructed for the required purposes, or it may be a general purpose computer selectively activated or configured by a computer program stored in the computer. In particular, various general purpose machines may be used with computer programs written in accordance with the teachings herein, or it may be more convenient to construct a more specialized apparatus to perform the required operations.

The invention can also be embodied as computer readable code on a computer readable medium. The computer readable medium is any data storage device that can store data which can be thereafter be read by a computer system. Examples of the computer readable medium include read-only memory, random-access memory, CD-ROMs, magnetic tape, optical data storage devices. The computer readable medium can also be distributed over a network coupled computer systems so that the computer readable code is stored and executed in a distributed fashion.

Although the foregoing invention has been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope and equivalents of the appended claims. *What is claimed is:*

Claims

1. A programming method for flashing a read only memory (ROM) chip of a host adapter with an updated BIOS code, the host adapter being connected to a host computer system, the method comprising:

5 building a table having start address information and memory size information of memory space occupied in the random access memory (RAM) of the host computer system by one or more PCI host adapters which are connected to the host computer system via a PCI bus;

identifying a selected PCI host adapter having a ROM chip;

10 mapping a desired amount of memory space for an updated option ROM code between the RAM of the host computer system and the ROM chip;

redirecting a start address in RAM of an additional PCI host adapter that is within the desired amount of memory space; and

15 loading the updated option ROM code into the desired amount of memory space in RAM and in the ROM chip of the selected host adapter.

2. A programming method for flashing a read only memory (ROM) chip as recited in claim 1, further comprising:

20 restoring the start address in RAM of the additional PCI host adapter after the loading of the updated option ROM code is complete.

3. A programming method for flashing a read only memory (ROM) chip as recited in claim 1, wherein before the redirecting is performed, the method further includes:

referring to the table to find start addresses that fall within the desired amount of memory space.

4. A programming method for flashing a read only memory (ROM) chip as  
5 recited in claim 3, wherein the desired amount of memory space begins at a start address of memory space in RAM that is used by the selected PCI host adapter.

5. A programming method for flashing a read only memory (ROM) chip as  
recited in claim 4, wherein the desired amount of memory space has a size necessary to fit  
10 the updated option ROM code, and the updated option ROM code is loaded beginning at the start address.

6. A programming method for flashing a read only memory (ROM) chip as  
recited in claim 1, wherein the redirecting is made to a temporary start address of zero.

15

7. A programming method for flashing a read only memory (ROM) chip as  
recited in claim 1, wherein the option ROM chip is an electrically erasable programmable  
read only memory (EEPROM) that can be flashed with the updated option ROM code during  
the loading.

20

8. A programming method for flashing a read only memory (ROM) chip as  
recited in claim 1, wherein the one or more PCI host adapters can include a SCSI host  
adapter and a redundant array of inexpensive disk (RAID) host adapter.

9. A method for programming a read only memory (ROM) chip of a host adapter that is connected to a computer system, comprising:

scanning for PCI host adapters being connected to the computer system;

5 building a table having start address information and memory size information of memory space occupied in random access memory (RAM) by the PCI host adapters that are connected to the computer system;

identifying a selected PCI host adapter having a ROM chip that is configured to be programmed with an updated option ROM code, the selected PCI host adapter being  
10 associated with a selected start address and a selected memory size;

mapping a desired amount of memory space for the updated option ROM code from RAM to the ROM chip;

identifying ones of the PCI host adapters having memory space in RAM in the desired amount of space beginning with the selected start address and extending for an  
15 update memory size;

re-directing start addresses of the ones of the PCI host adapters lying within the desired amount of space in RAM; and

loading the updated option ROM code into the desired amount of space in RAM and into the ROM chip.

20

10. A method for programming a read only memory (ROM) chip of a host adapter that is connected to a computer system as recited in claim 9, further comprising:

determining when the loading of the updated option ROM code is complete; and

when the loading is complete, restoring the start addresses of the ones of the PCI host adapters lying within the desired amount of space in RAM back to a state that is before the re-directing.

5        11.    A method for programming a read only memory (ROM) chip of a host adapter that is connected to a computer system as recited in claim 9, wherein the re-directing is performed for a temporary amount of time that is needed to complete the loading.

10       12.    A method for programming a read only memory (ROM) chip of a host adapter that is connected to a computer system as recited in claim 9, wherein the option ROM chip is an electrically erasable programmable read only memory (EEPROM) that can be flashed with the updated option ROM code during the loading.

15       13.    A method for programming a read only memory (ROM) chip of a host adapter that is connected to a computer system as recited in claim 9, wherein re-directing start addresses of the ones of the PCI host adapters lying within the desired amount of space in RAM comprises:

      setting the start addresses to zero.

20       14.    A method for programming a read only memory (ROM) chip of a host adapter that is connected to a computer system as recited in claim 9, identifying ones of the PCI host adapters having memory space in RAM in the desired amount of space further comprises:

referring to the table to ascertain if any of the PCI host adapters connected to the computer system have start addresses that lie within the desired amount of space.

15. A method for programming a read only memory (ROM) chip of a host adapter  
5 that is connected to a computer system as recited in claim 9, wherein the PCI host adapters can include a SCSI host adapter and a redundant array of inexpensive disk (RAID) host adapter.

16. A method for programming a read only memory (ROM) chip of a host adapter  
10 that is connected to a computer system as recited in claim 9, wherein the method of programming the ROM chip is part of a programming utility program.

17. A programming utility having program instructions for flashing a read only  
memory (ROM) chip of a host adapter with an updated BIOS code, the host adapter being  
15 connected to a host computer system, the programming utility comprising:

program instructions for building a table having start address information and  
memory size information of memory space occupied in the random access memory (RAM)  
of the host computer system by one or more PCI host adapters which are connected to the  
host computer system via a PCI bus;

20 program instructions for identifying a selected PCI host adapter having a ROM chip;

program instructions for mapping a desired amount of memory space for an updated  
option ROM code between the RAM of the host computer system and the ROM chip;



program instructions for redirecting a start address in RAM of an additional PCI host adapter that is within the desired amount of memory space; and

program instructions for loading the updated option ROM code into the desired amount of memory space in RAM and in the ROM chip of the selected host adapter.

5

18. A programming utility having program instructions for flashing a read only memory (ROM) chip of a host adapter with an updated BIOS code as recited in claim 17, further comprising:

program instructions for restoring the start address in RAM of the additional PCI host adapter after the loading of the updated option ROM code is complete.

10

19. A programming utility having program instructions for flashing a read only memory (ROM) chip of a host adapter with an updated BIOS code as recited in claim 17, wherein before executing the program instructions for redirecting, the utility further includes:

program instructions for referring to the table to find start addresses that fall within the desired amount of memory space.

15

20. A programming utility having program instructions for flashing a read only memory (ROM) chip of a host adapter with an updated BIOS code as recited in claim 19, wherein the desired amount of memory space begins at a start address of memory space in RAM that is used by the selected PCI host adapter.

20

21. A programming utility having program instructions for flashing a read only memory (ROM) chip of a host adapter with an updated BIOS code as recited in claim 20, wherein the desired amount of memory space has a size necessary to fit the updated option ROM code, and the updated option ROM code is loaded beginning at the start address.

5

22. A programming utility having program instructions for flashing a read only memory (ROM) chip of a host adapter with an updated BIOS code as recited in claim 17, wherein the redirecting is made to a temporary start address of zero.

10

23. A programming utility having program instructions for flashing a read only memory (ROM) chip of a host adapter with an updated BIOS code as recited in claim 17, wherein the programming utility is embodied in a computer readable media.

15

24. A method for flashing a read only memory (ROM) chip with an updated BIOS code, the method comprising:

building a table having start address information and memory size information of memory space occupied in a random access memory (RAM) of a host computer system by one or more host adapters which are connected to the host computer system;

identifying a selected host adapter having a ROM chip;

20 mapping a desired amount of memory space for an updated option ROM code between the RAM of the host computer system and the ROM chip;

redirecting a start address in RAM of an additional host adapter that is within the desired amount of memory space; and

loading the updated option ROM code into the desired amount of memory space in RAM and in the ROM chip of the selected host adapter.

25. A method for flashing a read only memory (ROM) chip as recited in claim 24,  
5 further comprising:

restoring the start address in RAM of the additional host adapter after the loading of the updated option ROM code is complete.

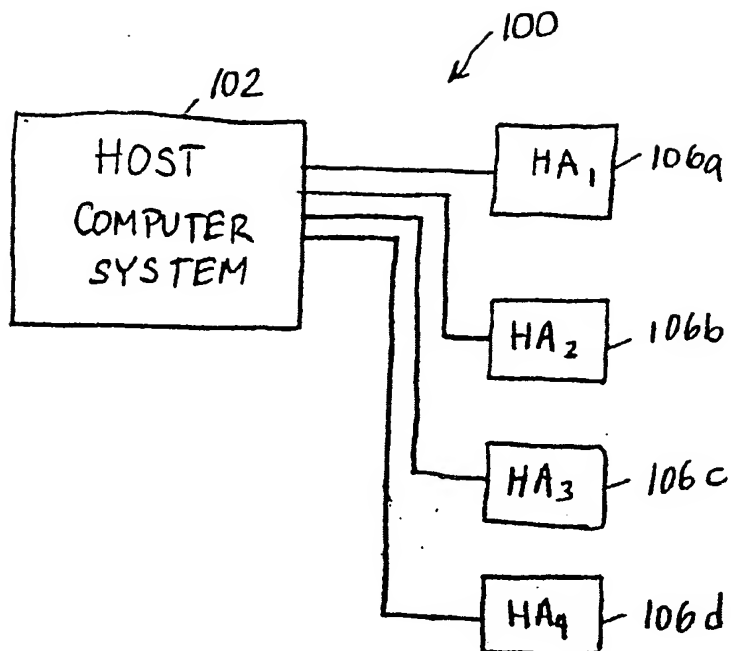


FIG. 1A

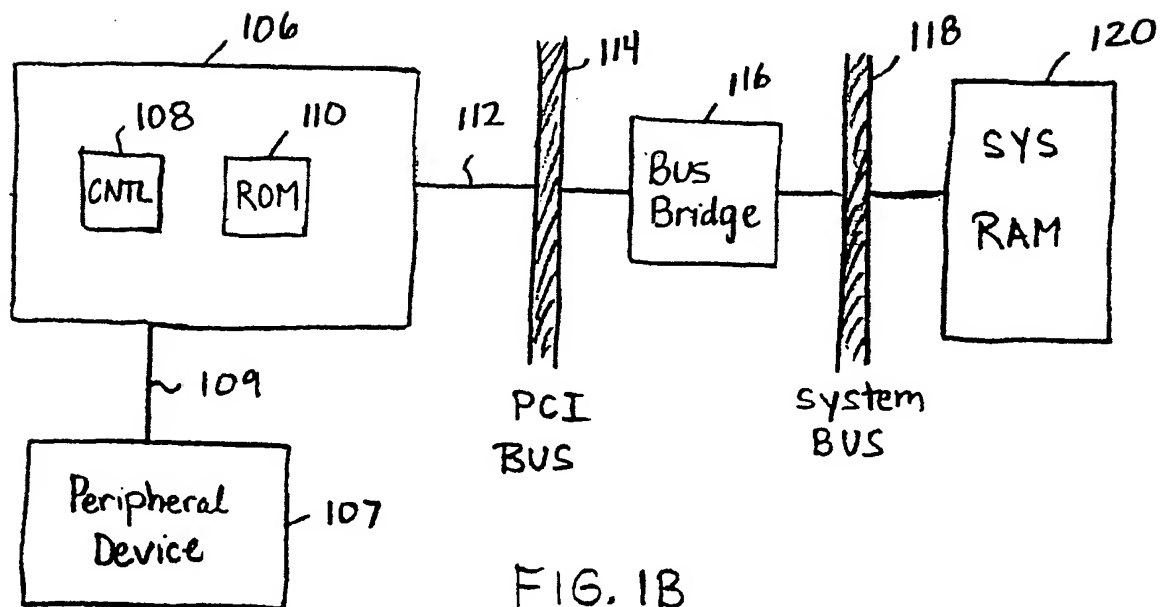


FIG. 1B

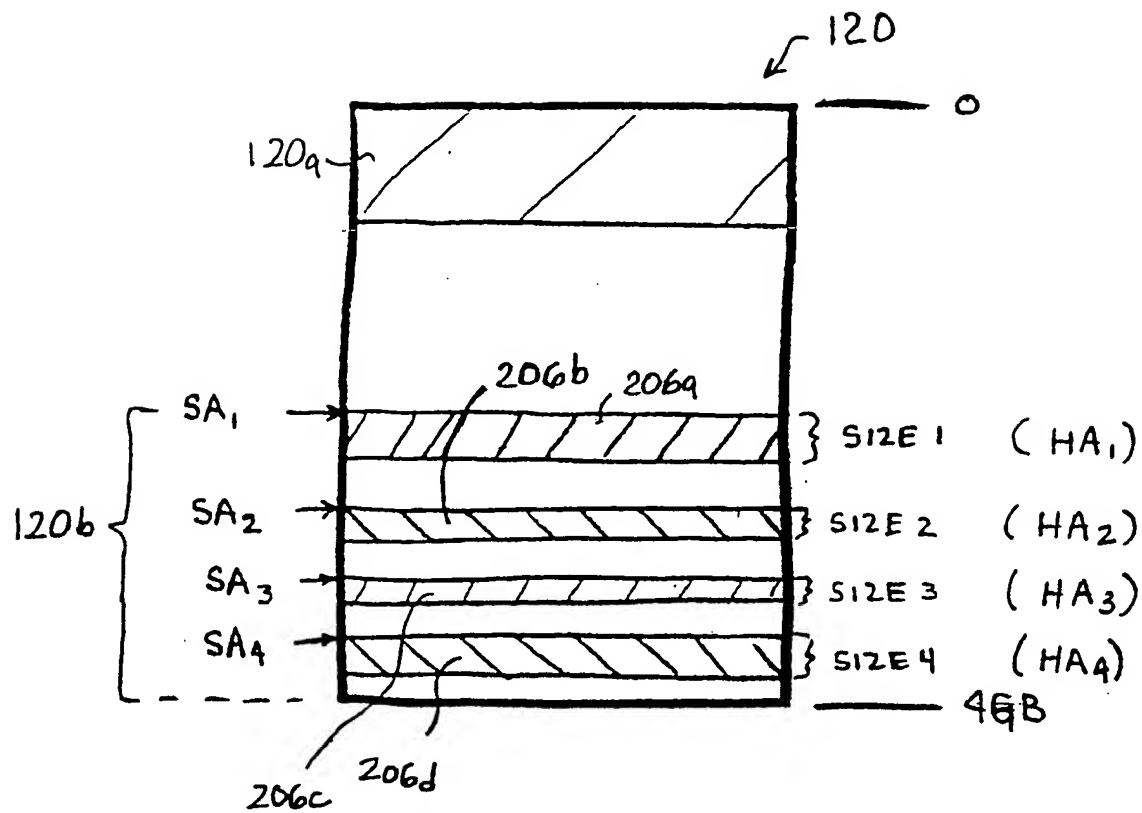


FIG. 2

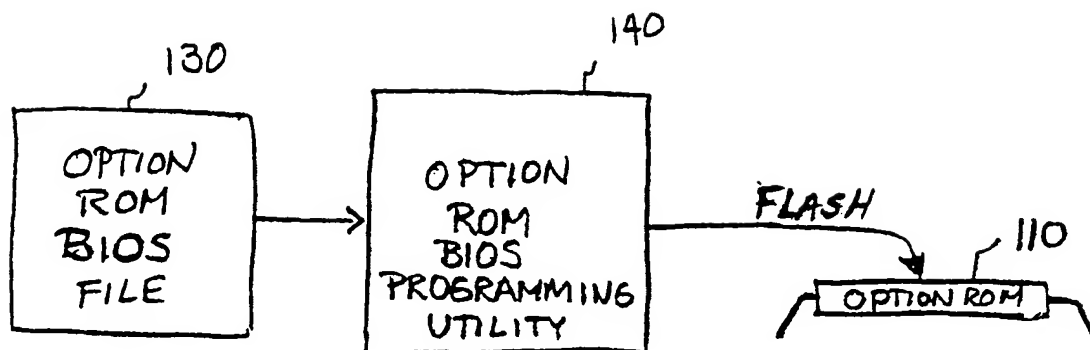


FIG. 3

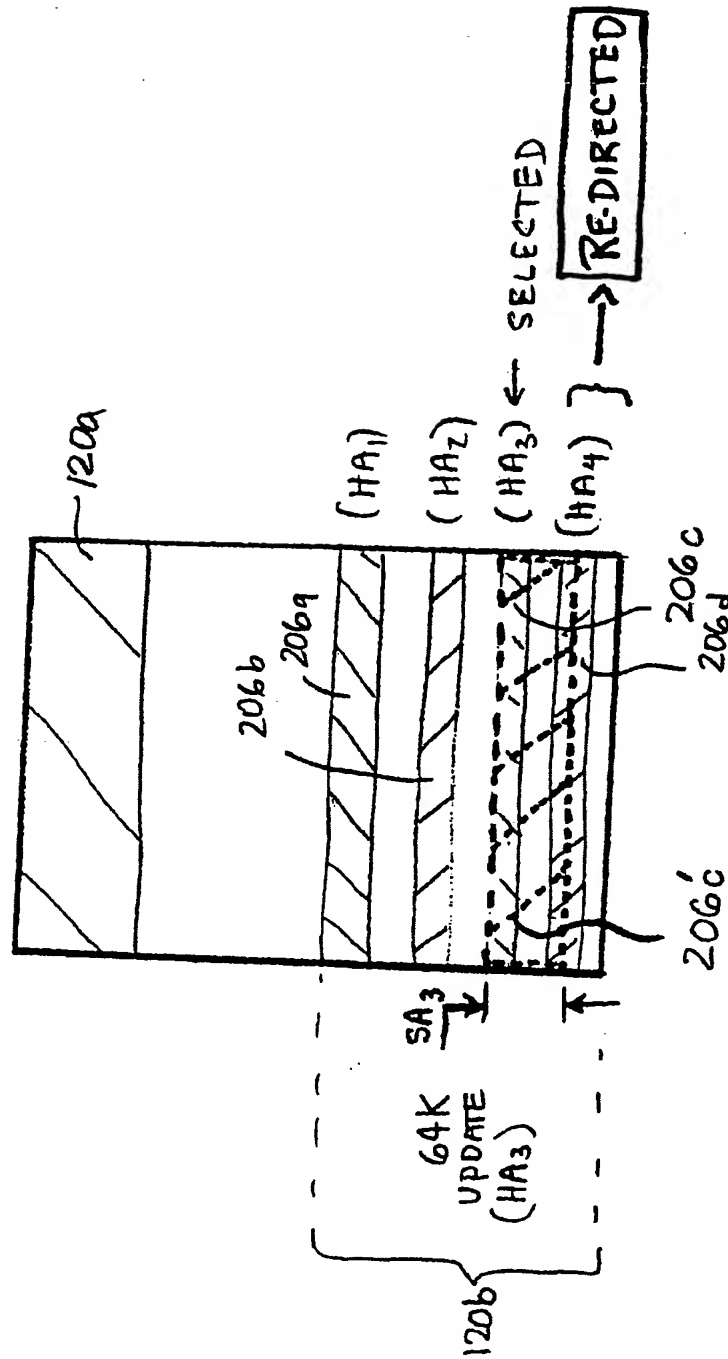


FIG. 4

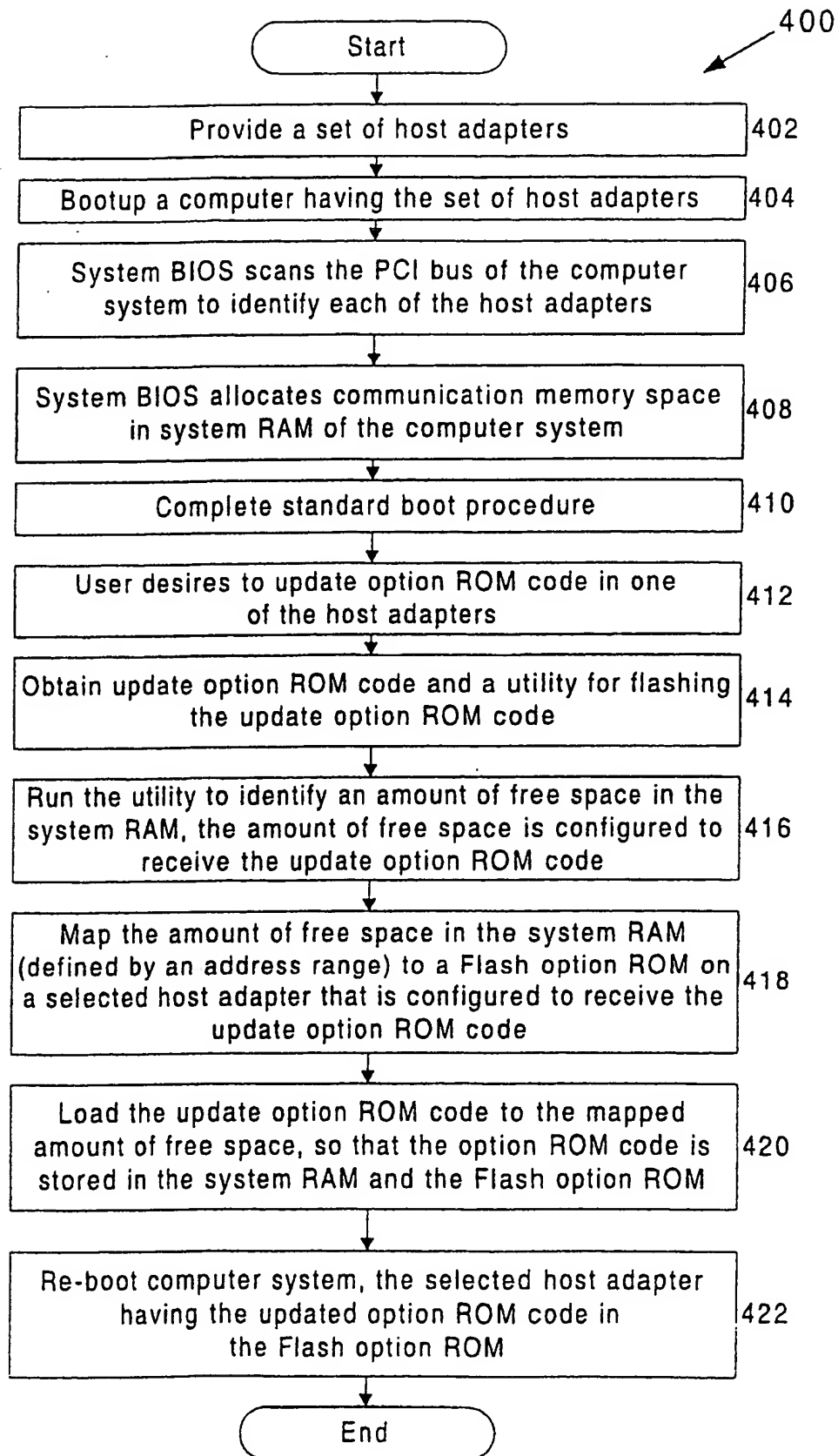


FIG. 5

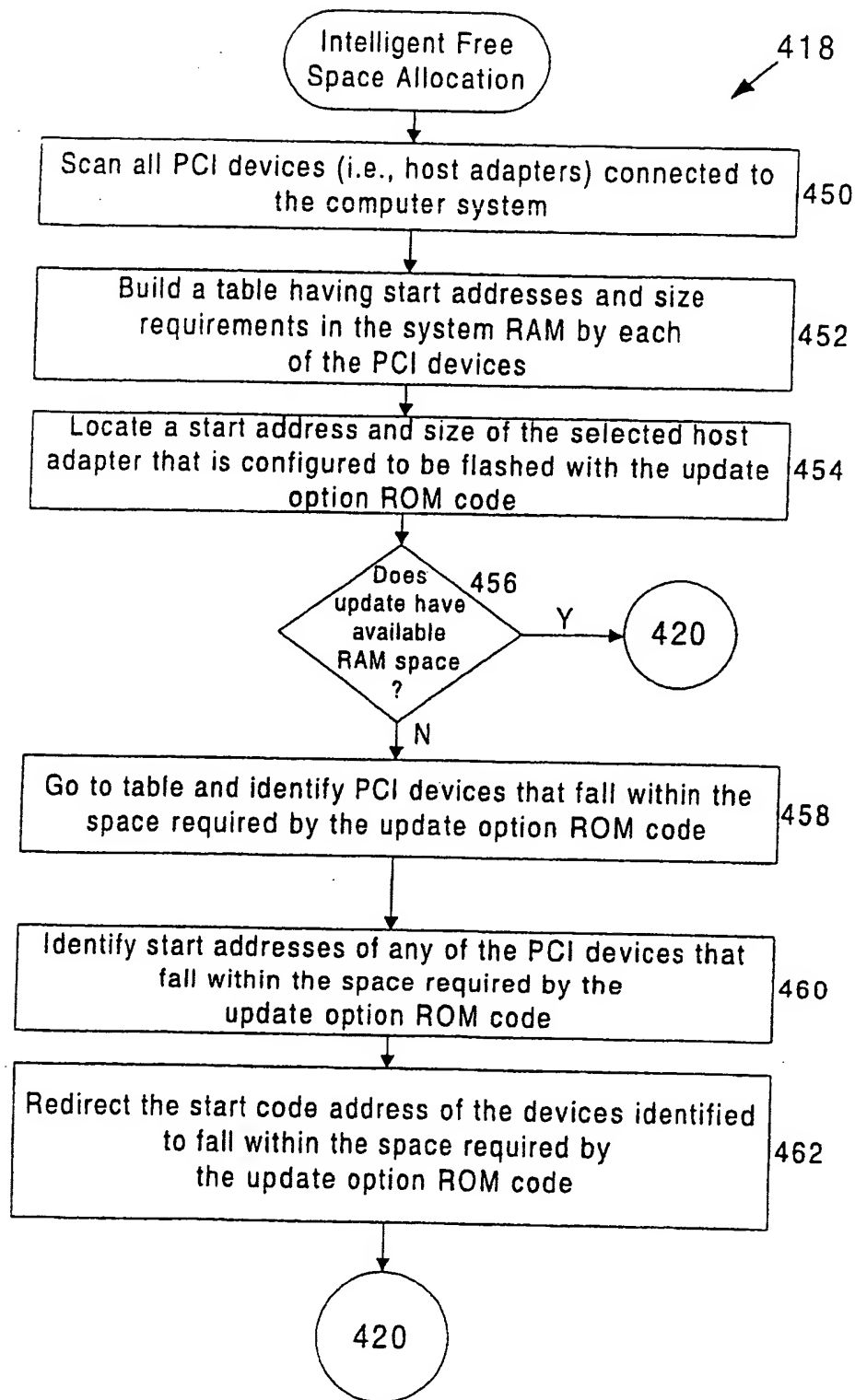


FIG. 6



SELECTED  
HA  
↓

	HA <sub>1</sub>	HA <sub>2</sub>	HA <sub>3</sub>	HA <sub>4</sub>
START ADDRESS	SA <sub>1</sub>	SA <sub>2</sub>	SA <sub>3</sub>	SA <sub>4</sub>
SIZE	SIZE <sub>1</sub>	SIZE <sub>2</sub>	SIZE <sub>3</sub>	SIZE <sub>4</sub>

FIG. 7A

SELECTED  
HA  
↓

	HA <sub>1</sub>	HA <sub>2</sub>	HA <sub>3</sub>	HA <sub>4</sub>
START ADDRESS	SA <sub>1</sub>	SA <sub>2</sub>	SA <sub>3</sub>	0
SIZE	SIZE <sub>1</sub>	SIZE <sub>2</sub>	SIZE <sub>3</sub> (6K)	SIZE <sub>4</sub>

↙ 302

FIG. 7B

## INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US00/13893

## A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : Please See Extra Sheet.

US CL : Please See Extra Sheet.

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : Please See Extra Sheet.

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched  
FOLDOC Online Computer DictionaryElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)  
Please See Extra Sheet.

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JEX, J. Flash Memory BIOS for PC and Notebook Computers, Communications, Computers and Signal Processing, 1991., IEEE Pacific Rim Conference on , 1991, Vol. 2, pp. 692-695.	1-25
A	KRAMER, A. et al. Ultra-Low-Power Analog Associative Memory Core Using Flash-EEPROM-Based Programmable Capacitors, Proceedings 1995 International Symposium on Low Power Design, 1995, pp. 203-208.	1-25
Y, P	SUDARSANAM, A. et al. Simultaneous Reference Allocation in Code Generation for Dual Data Memory Bank ASIPs, ACM Trans. Des. Autom. Electron. Syst. Vol. 5, No. 2, April 2000, pp. 242-264.	1-25

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents	* T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
* A* document defining the general state of the art which is not considered to be of particular relevance	* X* document of particular relevance, the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
* E* earlier document published on or after the international filing date	* Y* document of particular relevance, the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
* L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	* &* document member of the same patent family
* O* document referring to an oral disclosure, use, exhibition or other means	
* P* document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 05 OCTOBER 2000	Date of mailing of the international search report 26 OCT. 2000
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer THOMAS LEE Telephone No. (703) 305-9717

## INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US00/13893

## C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	QIU, X. et al. Options for Dynamic Address Translation in COMAs, Proceedings of the 25th Annual International Symposium on Computer Architecture, 1998, pp. 214-225.	1-25
A, P	OHMI, T. et al. Association Hardware for Intelligent Electronic Systems, Systems and Computers in Japan, Vol. 30, Issue: 12, November 1999, pp. 52-62.	1-25
Y	US 5,167,030 A (SPILO) 24 November 1992, see entire document, especially figure 9.	1-25
Y	US 5,237,669 A (SPEAR et al) 17 August 1993, see entire document, especially figures 13 and 14.	1-25
Y	US 5,142,667 A (DIMPERIO et al.) 25 August 1992, see entire document, especially col. 17, lines 3-20.	1-25
Y	US 5,371,876 A (EWERTZ et al.) 6 December 1994, see entire document, especially figure 3A.	1-25
A	US 5,444,664 A (KURODA et al.) 22 August 1995, see entire document.	1-25
Y	US 5,479,639 A (EWERTZ et al.) 26 December 1995, see entire document, especially figure 8.	1-25
Y	US 5,550,997 A (IP et al.) 27 August 1996, see entire document, especially figures 8 and 21-24.	1-25
A	US 5,757,690 A (McMAHON) 26 May 1998, see entire document.	1-25
Y	US 5,815,722 A (KALWITZ et al.) 29 September 1998, see entire document, especially figures 21-24.	1-25
Y	US 5,841,991 A (RUSSELL) 24 November 1998, see entire document, especially figures 21-24.	1-25
Y, P	US 5,933,652 A (CHEN et al. 03 August 1999, see entire document, especially figure 1.	1-25
A, P	US 5,987,536 A (JOHNSON et al.) 16 November 1999, see entire document.	1-25

# INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US00/13893

## A. CLASSIFICATION OF SUBJECT MATTER. IPC (7)

G06F 12/02, 9/06, 11/00, 11/22, 11/28, 11/34, 12/00, 12/12, 12/16, 13/00, 13/10, 13/14, 13/16, 15/02, 15/177, G11C 13/00, 17/00; G06K 15/00

## A. CLASSIFICATION OF SUBJECT MATTER: US CL

710/36, 3, 5, 10, 14, 26, 74, 129; 705/405; 709/104, 107, 108, 200, 216, 221, 222, 310; 711/159, 2, 4, 103, 111, 112, 114, 134, 136, 152, 154, 155, 160, 163, 170, 173, 201, 203, 209; 713/1, 2; 714/5, 8, 38; 717/11; 365/104, 226

## B. FIELDS SEARCHED

Minimum documentation searched  
Classification System: U.S.

710/36, 3, 5, 10, 14, 26, 74, 129; 705/405; 709/104, 107, 108, 200, 216, 221, 222, 310; 711/159, 2, 4, 103, 111, 112, 114, 134, 136, 152, 154, 155, 160, 163, 170, 173, 201, 203, 209; 713/1, 2; 714/5, 8, 38; 717/11; 365/104, 226

## B. FIELDS SEARCHED

Electronic data bases consulted (Name of data base and where practicable terms used):

USPT, EPAB, JPAB, DWPI, TDBD, iTKnowledge.com, ACM Digital Library, IEEE Xplore, Wiley InterScience  
search terms: temporarily, redirect, load, reallocate, update, transfer, swap, retrieve, ROM, memory, RAM, EEPROM, PCI, BIOS, operating system, program, code, map, displaced, occupied, space, flash memory, modify, rewrite, computer, PC